Remarks

Claims 2 - 6 and 8 - 15 are pending. Favorable reconsideration is respectfully requested.

The present invention is directed to an improved process for producing silicon wafers having an epitaxial layer thereon. With increasingly tight design rules for semiconductor products such as integrated circuits, silicon wafer defects of sizes which were easily tolerated by more relaxed design rules are now severe obstacles to producing wafers which can be used with the newest generation of design rules without significant numbers of failed devices. The problem is severe enough that the use of epitaxially coated wafers is markedly increasing, despite the cost penalty associated with their use. However, even epitaxially deposited layers cannot, in some cases, compensate for too large or too many surface defects on the wafers onto which the epitaxial layers are deposited.

In addition to the problems discussed above, the cost of silicon wafers is already high, not only due to the high costs associated with very pure raw materials and single crystal ingot growth, i.e. by the Czochralsky method, but also due to the multiplicity of grinding, edge contouring, lapping, etching, and polishing steps required. Polishing, for example, and as indicated by Sakata EP 0 711 854, conventionally involves three distinct polishing steps, each producing a finer and more defect-free surface than the previous step.

Applicants have discovered that epitaxial wafers can be produced more economically and yet have fewer localized light scattering defects (inclusive of but not limited to COPs) when the surface of the wafer to be epitaxially coated is subjected to only a single material removing polishing step, which preferably produces a surface having an RMS roughness of 0.05 to 0.29 nm, followed by a <u>two stage</u> pre-epitaxy thermal treatment, the first stage of which takes place in hydrogen gas containing no effective amount of HCl etchant, and the second of which takes place in a mixture of H_2 and HCl, the HCl being present in an amount such that the etching rate in the second stage, at the thermal treatment temperature, is

from 0.01 to 0.1 μm/min, and 0.01 to 0.2 μm of material is removed from the wafer surface. Applicants have surprisingly discovered that the two step combination results in material being removed in the second step in a preferential manner as opposed to non-preferential etching disclosed by the prior art using a single H_2/HCl mixture in a one stage process.[1] As a result, wafers with exceptionally low levels of defects are produced, despite elimination of several expensive and time consuming polishing steps.

Claim 2, the broadest independent claim, has been amended to make the process steps clear. It was not apparent from the prior claims that the H_2/HCl treatment was in fact a two stage treatment, the first in H_2 to remove oxide, and the second in H_2 and HCl. The second step can be performed not only by physically introducing HCl directly into the reactor, but also by first evacuating hydrogen from the reactor and replacing it with a mixture of H_2/HCl, flushing hydrogen from the reactor and introducing H_2/HCl, or any equivalent process, so long as the first step is practiced with hydrogen containing substantially no HCl. Support for the amendments to claim 2 may be found in the second paragraph of page 6, the last paragraph of page 7, page 11, last line to page 12, 4th to last line, and the Example on pages 17 and 18. Thus, no new matter is introduced by virtue of this amendment.

New claims 12 - 15 have been added. Support may be found in the specification, including the claims as originally filed. Thus, no issue of new matter arises by virtue of the presentation of the new claims.

Claims 2 - 6, 8, and 11 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Fujikawa et al. U.S. Patent No. 6,261,362 ("*Fujikawa*") in view of Sakata et al. published application EP 0 711 854 (*Sakata*), and Liaw et al. ("*Liaw*"). Applicants respectfully traverse this rejection as first, *Fujikawa* and *Sakata* are not properly combinable;

[1] The preferential removal of material may actually be a combined removal of material in conjunction with deposition of material in low lying areas, as discussed in the specification on page 6. Regardless of the actual mechanism, the result is preferential removal of elevated features and not non-preferential removal.

and second, the combination of *Fujikawa, Sakata,* and *Liaw* does not teach or suggest the claimed invention.

Fujikawa is directed to a method of decreasing the size of COP defects and also decreasing their number, by growth of crystals having a large carbon concentration. *Fujikawa* teaches that COP size decreases with increasing pull rate while COP density increases with increasing pull rate when carbon concentration is normal. By significantly increasing carbon content (Figs. 2, 3), both COP size and density may both be lowered at a given pull rate. *Fujikawa* discloses that wafers produced from this process may be subjected to multiple stage polishing and then epitaxially coated to produce wafers suitable for design rules as low as 0.18 μm. *Fujikawa* does not disclose, nor does he teach or suggest that a single polishing step might be useful, despite single polish/epitaxy treatments proposed earlier, and published in JP 279515/94 (*Sakata EP 0 711 854 A1).* Prior to depositing the epitaxial layer, the silicon wafers are etched in H_2/HCl at an unspecified etching rate, at 1150°C for 100 sec, followed by epitaxial deposition.

Sakata is directed to preparation of epitaxial wafers, and states that multiple stage polishing should be avoided, and should be replaced by a single (haze) polish which results in a surface roughness (RMS, 1 μm x 1 μm) of 0.3 nm to 1.2 nm. *Sakata* then epitaxially deposits silicon directly onto the surface. No H_2/HCl pretreatment is described.

Liaw teaches that H_2 treatment of wafers prior to epitaxy is known, and that etching with H_2/HCl is also known as an alternative. *Liaw* is clear that these treatments are alternative choices: "The choice of H_2 or HCl for prebake. . ." *See*, in general, the 2nd full paragraph of page 73 of *Liaw*. *Liaw* also teaches that when H_2/HCl treatment is used, that the wafer surface is nonpreferentially etched. In other words, if peaks and valleys existed prior to etching, peaks and valleys of the same relative height will exist following etching; the valleys will be etched at the same rate as the peaks - nonpreferentially.

Applicants respectfully submit that *Fujikawa* and *Sakata* are not properly combinable. In the case of *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999), the CAFC has indicated that the requirement for showing the teaching or motivation to combine references is "rigorous." *Dembiczak* at 1617. Moreover, this showing, which is rigorously required, must be "clear and particular." *Dembiczak* at 1617. See also, *C.R. Bard v. M3 Sys., Inc.*, 48 U.S.P.Q.2d 1225, 1232 (Fed. Cir. 1998). It is well established that merely because references can be combined, the mere suitability for logical combination does not provide motivation for the combination. See, *Berghauser v. Dann, Comr. Pats.*, 204 U.S.P.Q. 398 (DCDC 1979); *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 221 U.S.P.Q. 929 (Fed. Cir. 1984). Moreover, mere conclusory statements supporting the proposed combination, standing alone are not "evidence". *McElmurry v. Arkansas Power & Light Co.*, 27 U.S.P.Q.2d 1129, 1131 (Fed. Cir. 1993). *See also, In re Lee*, 61 U.S.P.Q. 2d 1430 (Fed. Cir. 2002).

Here, *Fujikawa* discloses only multiple stage polishing, while *Sakata* prohibits multiple stage polishing. These references thus have entirely opposing disclosures and one skilled in the art would not be motivated to combine them for this reason. Furthermore, there is no evidence of record which supports the combination, as required by *Dembiczak*. It is very unlikely that *Fujikawa* was not aware of *Sakata*, a published application of a known competitor in the same country, yet *Fujikawa* does not teach or suggest using the single stage polishing of *Sakata*, instead resorting to a more complicated crystal growth process incorporating high amounts of carbon into the crystal lattice. This is strong evidence that one skilled in the art would not be motivated to combine these references. If the Office disagrees, it must supply evidence which would direct the skilled artisan to combine these references. The rejection over *Fujikawa* in view of *Sakata* and *Liaw* should be withdrawn for this reason alone.

Moreover, even if combination were proper, the combination does not teach or suggest the claimed subject matter, whether with or without *Liaw*.

Fujikawa teaches only etching his multiple stage, fully polished wafers with a mixture of H_2/HCl, and not a two stage process as claimed. Moreover, *Fujikawa* does not disclose any etching rate, nor does *Fujikawa* disclose any depth of material removed. *Sakata* does not supply these deficiencies, since *Sakata* does not suggest any pretreatment prior to epitaxy. *Liaw* also does not supply these defects, as *Liaw* teaches that H_2 and H_2/HCl treatments are alternatives and does not teach or suggest that they be used sequentially. That the order is important is indicated by the present, presumptively accurate specification. *Liaw* describes H_2/HCl etching as nonpreferential, while in the present process, as indicated in the specification, H_2/HCl etching following H_2 treatment to remove oxide is preferential, attacking the peaks and leveling the surface. At page 73, first paragraph, *Liaw* discloses that H_2/HCl etching is effective at eliminating "spikes and stacking faults" in the later epitaxy. This is not at all the same as preferential etching, and in fact is totally unrelated. Applicants' process reduces the RMS values of surface roughness by preferential etching, pre-epitaxy.

Finally, *Liaw* does not disclose any etching rate. *Liaw* does disclose a hydrogen prebake to remove oxide, such a prebake extending for 10 minutes (page 71). However, this would pertain only to Applicants first thermal treatment. With respect to the H_2/HCl etch, *Liaw* discloses that removal of 0.1 to 0.5 μm produces a "clean and damage free" surface, i.e. removal of subsurface mechanical damage from polishing (but no mention of defects such as COPs). However, there is no disclosure with regard to etching rates.[2] By direct comparative examples (Comp. Ex. 2) a wafer processed at a higher etch rate of 2 μm/min with a total

[2] The Office states that the claimed etching rate is established by *Fujikawa*'s treatment for 100 seconds to remove 0.1 to 0.5 μm of material (taught by *Liaw*). This is incorrect, for *Fujikawa* does not disclose any amount of material removed. *Liaw* discloses that 0.1 μm to 0.5 μm is conventional. However, the wafers of *Fujikawa* are not conventional, but are specially manufactured to have high carbon content. It is not known whether a greater or lesser amount of material would be necessitated to be removed than the amount suggested by *Liaw*. For example, *Fujikawa* may have removed 1 μm of material, which would be a very high etching rate of 0.6 μm/min. To guess at how much *Fujikawa* removed over the 100 second period is pure speculation, which cannot be used in rejecting the claims. None of the references teach or suggest that an etching rate of 0.01 to 0.1 μm/min be used. Factually, none of the references or any combination teach or suggest any etching rate.

removal of 2 μm silicon produced a concentration of LLS defects some 7 times higher than the claimed process. By removing 2 μm of silicon, one would have expected a very high quality surface. However, the surface is inferior to those of the claimed process because the etch rate is too high.

Finally, *Sakata* teaches that its wafers have a surface roughness of 0.3 nm to 1.2 nm RMS. Applicants' new claims 12 - 15 require a surface roughness of 0.05 to 0.29 nm RMS. *Sakata* does not teach or suggest using wafers with a lower surface roughness, and Applicants have shown, by direct comparative example (Comp. Ex. 1), that a wafer of 0.7 nm RMS roughness, squarely within the range of *Sakata*, and not subject to pretreatment (*Sakata* also does not pretreat), produces epitaxial wafers with 15 times higher LLS defects than when the claimed invention is used.

As none of the references, alone or in conjunction, teach a two stage thermal treatment, the first stage with hydrogen and the second with H_2/HCl; and as none of the references teach or suggest, alone or in combination, the claimed etching rate, withdrawal of the rejection over *Fujikawa* in view of *Sakata* and *Liaw* is solicited for this reason also.

Claims 9 and 10 have been rejected under 35 U.S.C. § 103(a) over *Fujikawa* in view of *Sakata* and *Liaw* and further in view of Fabry et al. U.S. Patent 5,219,613 ("*Fabry*"). As the combination of *Fujikawa*, *Sakata,* and *Liaw* does not render the broader claims obvious, the addition of *Fabry*, for the purpose of teaching the additional oxidizing, hydrophillizing step of claims 9 and 10 cannot render these claims obvious. Withdrawal of the rejection under 35 U.S.C. § 103(a) over *Fujikawa* in view of *Sakata, Liaw,* and *Fabry* is solicited.

Applicants submit that the claims are now in condition for Allowance, and respectfully request a Notice to that effect. If the Examiner believes that further discussion will advance the prosecution of the Application, the Examiner is highly encouraged to telephone Applicants' attorney at the number given below.

Respectfully submitted,

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Date: June 9, 2005

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